PATENT ABSTRACTS OF JAPAN

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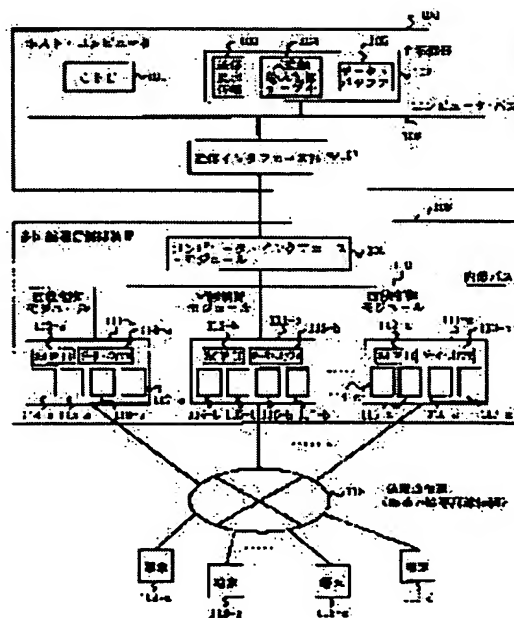ONO SHUJI
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(54) MULTIPLE ADDRESS COMMUNICATION SYSTEM

(57)Abstract:

PURPOSE: To avoid an overhead for multiple address communication processing when data cannot be sent to a line due to a fault of the line in the case of data transmission by providing two kinds of queue tables for 1:1 communication and for multiple address communication to a line control module.
CONSTITUTION: In the computer system in which a host computer 100 and plural terminal equipments) 119-a-119-d) are interconnected by plural lines via at least two data buffers 105,113 (113-a-113-c) or over, two kinds of queue tables for 1:1 communication 114 (114-a-114-c) and for multiple address communication 115 (115-a-115-c) are provided to a line control module 111 (111-a-111-c) managing the buffer 113 closest to the line. In the case of multiple address communication, when the queue table 115 of the module 111 is fully occupied, a CPU 101 stops registration of a data transmission request. Then data are sent again to a terminal equipment to which data transmission is not finished through one to one communication after the end of multiple address communication.

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